
DigiRadio

DAB+/FM Bluetooth Receiver
with SigmaDSP Audio Processing

Technical Reference Manual

v1.0 (pre-prototype)



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Open-Source Hardware Project

Manufactured with PCBWay — 6-layer, impedance-controlled

Licensed under CERN-OHL-S (hardware) and MIT (firmware)

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Chapter 1

Overview

1.1 Introduction

DigiRadio is an open-source digital radio receiver that combines terrestrial broadcast reception (**DAB+** / **DAB** / **FM**) with a programmable audio-processing stage and high-quality **Bluetooth** audio output. Incoming broadcast audio is decoded by a Silicon Labs Si4684 digital-radio receiver, processed by an Analog Devices ADAU1701 SigmaDSP (equalisation, mixing, level control), and transmitted over Bluetooth by a Qualcomm QCC3056-based FSC-BT1035 module supporting the **aptX Adaptive** codec. An Espressif ESP32-S3 acts as the host controller, orchestrating the three subsystems and providing Wi-Fi/BLE connectivity and a USB service interface. The tuner→DSP→Bluetooth path is fully digital (I²S, 48 kHz / 24-bit).

1.2 Key Features

- DAB+ / DAB / FM reception (Si4684) via external whip antenna (SMA).
- Fully digital audio path (I²S, 48 kHz / 24-bit).
- Programmable audio processing on the ADAU1701 SigmaDSP.
- Bluetooth 5.2 output with aptX / aptX HD / **aptX Adaptive**.
- ESP32-S3 host with native USB, Wi-Fi and BLE.
- USB-C powered; 3.3 V main rail + low-noise 1.8 V for the tuner.
- 6-layer impedance-controlled PCB, 50 × 90 mm, two ground planes.
- Three antennas (ESP32 2.4 GHz, BT1035 2.4 GHz, FM/DAB SMA) with keep-outs.

Design Decision

The design goal was *sound quality first* for the wireless link. Because the final DAC lives in the Bluetooth sink, the codec is the single most important quality factor in the chain. The QCC3056/aptX Adaptive path was chosen over cheaper SBC/AAC-only modules, and the whole tuner→DSP→BT path is kept digital to avoid any avoidable A/D–D/A conversion.

Chapter 2

System Architecture

2.1 Signal Chain

The audio signal flows entirely in the digital domain from tuner to Bluetooth module (Figure 2.1).

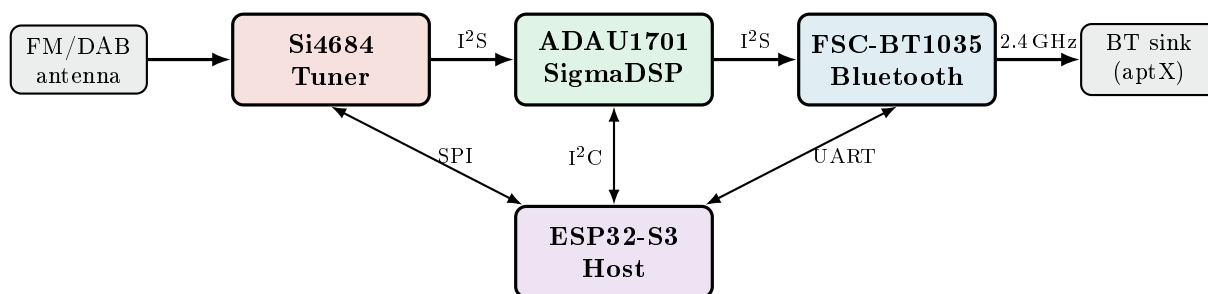


Figure 2.1: Signal chain. Audio (top) stays digital end-to-end; the ESP32-S3 host (bottom) controls each subsystem over its own bus.

Note

The ESP32-S3 can inject its own audio stream (e.g. Wi-Fi internet radio or prompts) into the DSP over a second I²S input, letting the DSP mix broadcast and network audio before the Bluetooth stage.

2.2 Clock Architecture

The I²S bus is driven by a single master. The ADAU1701 is the I²S **master**, generating BCLK and LRCLK from its 12.288 MHz crystal ($12.288 \text{ MHz} / 256 = 48 \text{ kHz}$). The Si4684 and FSC-BT1035 are I²S slaves. The Si4684 keeps its own independent 19.2 MHz reference crystal for RF synthesis.

Design Decision

The ADAU1701 was made I²S master because it already carries a 12.288 MHz crystal that divides cleanly to 48 kHz ($\times 256$). Making the BT module master would have forced the DSP PLL to lock to an incoming LRCLK of possibly 44.1 kHz, introducing a sample-rate mismatch (the ADAU1701 has no ASRC). With the DSP as master, both tuner and BT module follow its clean 48 kHz.

2.3 Power Tree

The board is powered from USB-C (5 V). A buck converter generates the 3.3 V rail; a low-noise LDO derives the 1.8 V rail required by the Si4684 analogue and memory supplies (Figure 2.2).

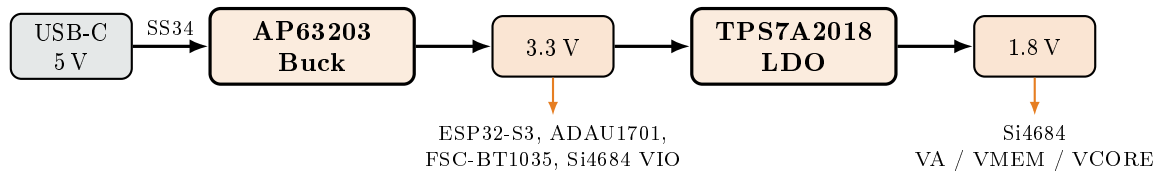


Figure 2.2: Power tree. A single series Schottky (SS34) protects the USB input; the buck feeds all 3.3 V loads, and the LDO provides the quiet 1.8 V rail for the tuner.

Important

The Si4684 requires 1.8 V (not 3.3 V) on VA, VMEM and VCORE; only VIO may be 1.8–3.6 V and is set to 3.3 V here so that SPI and I²S logic levels match the ESP32 and DSP domains.

Chapter 3

Functional Blocks

3.1 RF Front-End — Si4684 Digital Radio Receiver

The Si4684-A10-GM (QFN-48) receives FM, DAB and DAB+ from an external whip antenna through an SMA edge connector. The design follows Silicon Labs application note **AN851** for the schematic and layout of the RF input and supply bypassing.

3.1.1 Supplies and Sequencing

VA, VMEM and VCORE run from the 1.8 V rail; VIO runs from 3.3 V to match the host logic. SMODE is tied low to select the SPI control bus, over which the ESP32-S3 loads the tuner firmware/patch image at boot. RSTB is held low during supply ramp and released by the host only after both rails are stable.

Important

During the SPI firmware download the chip-select (**SSB**) must be held low for the entire transaction — it must not toggle between bytes. On the ESP32-S3, **SSB** is therefore driven as a software-controlled GPIO, not by the SPI peripheral's automatic chip-select.

3.1.2 Supply Bypassing (AN851)

Each supply pin (VA, VMEM, VCORE, VIO) carries a decoupling triplet of 8.2 pF (C0G), 2.2 nF and 1 μ F. Per AN851 these bypass capacitors return to the internal bypass nodes DBYP / ABYP, *not* to the general ground plane; DBYP and ABYP are internal-regulator/return nodes and are not tied to GND.

Design Decision

This is the single most non-obvious detail of the Si468x. Applying the generic “cap-to-ground” decoupling rule here would be wrong: AN851 explicitly routes the supply bypass capacitors to DBYP/ABYP to keep the receiver's reference quiet. On the PCB each triplet is placed against its own pin, smallest value nearest the pin, with the return via immediately after the capacitor.

3.1.3 RF Matching and Protection

The FM/DAB matching network (whip-antenna topology) comprises a 33 pF DC-blocking capacitor, an 18 nH series inductor, a 2.7 pF shunt (C0G), and 120 nH / 22 nH tuning inductors into VHFI/VHFSW. A BAV99 dual diode provides bidirectional ESD clamping: its common node sits on the RF line and both ends return to ground, presenting the minimum shunt capacitance to the antenna.

3.1.4 Reference Crystal

A 19.2 MHz crystal (10 pF CL) with two 12 pF C0G load capacitors provides the RF reference. The crystal and its load caps are placed with a minimal loop against XTALI/XTALO, guarded by ground and with an unbroken ground plane beneath.

3.2 Audio DSP — ADAU1701 SigmaDSP

The ADAU1701JSTZ-RL (LQFP-48) performs equalisation, mixing and level control. It receives audio from the Si4684 (SDATA_IN0) and from the ESP32-S3 (SDATA_IN1), and outputs to the Bluetooth module (SDATA_OUT0).

3.2.1 Clocking and I²S Role

The DSP is the I²S master, clocked by a 12.288 MHz crystal (two 22 pF C0G load caps). PLL_MODE0 and PLL_MODE1 are both tied low for the $256 \times f_s$ ratio (12.288 MHz / 48 kHz = 256). VDRIVE and IOVDD are at 3.3 V so the digital outputs match the host logic. The PLL loop filter uses 475Ω / 3.3 nF / 56 nF per the datasheet.

3.2.2 Program Loading

The design uses the **host-load** model: SELFB00T is tied low, and the ESP32-S3 writes the compiled SigmaStudio program into the DSP RAM over I²C at boot (halt core, write program/parameter RAM, restart). The on-board self-boot EEPROM is an optional (unpopulated) footprint.

Design Decision

Two decisions here came out of design review. First, host-load was chosen over self-boot so the ESP32 is the sole I²C master and also controls the DSP at runtime — eliminating the two-master contention that self-boot would create. Second, an early revision wired the DSP control port only to its self-boot EEPROM and *not* to the system I²C bus; that would have left the host unable to change volume/EQ at runtime. The port is now on the shared system bus.

3.2.3 Control Interface

The DSP control port sits on the system I²C bus (2.2 k Ω pull-ups). CLATCH/WP is tied to a defined level for I²C mode; ADDR0/ADDR1 set the slave address. The reset line is driven by the host (GPIO47) with a 10 k Ω pull-up and a small POR capacitor.

3.3 Bluetooth — FSC-BT1035 (QCC3056)

The FSC-BT1035 is a Bluetooth 5.2 audio module built on the Qualcomm QCC3056, supporting A2DP/AVRCP/HFP and the aptX / aptX HD / **aptX Adaptive** codecs. In DigiRadio it operates as an **A2DP source**, taking the processed I²S stream from the DSP and transmitting it to a Bluetooth sink.

- **I²S slave:** PCM_CLK=BCLK, PCM_SYNC=LRCLK, PCM_IN=SDATA_OUT0 from the DSP.
- **Power-on:** SYS_CTRL (host GPIO15, pull-down) asserts to power the module on; RESET (host GPIO17) relies on the module's internal pull-up.
- **Control:** UART with the Feasycom ASCII command set (4-wire, flow control).
- **Supplies:** VBAT_IN = 3.3 V, VDD_IO = 3.3 V, 1.8V_OUT bypassed only.

- **Firmware/role:** requires the Audio-Transceiver (source-capable) firmware in Host mode.

Note

The FSC-BT1035 is MSL-3 rated and must be baked before reflow. The PCB footprint uses the pin-compatible BT806 land pattern.

3.4 Host — ESP32-S3-WROOM-1

The **ESP32-S3-WROOM-1-N16** host provides Wi-Fi, BLE, native USB and control of all three sub-systems. Native USB (GPIO19/20) handles programming and console, freeing UART0 for a system-monitor header (CN1). UART1 (with flow control) drives the FSC-BT1035. SPI controls the Si4684; the system I²C controls the DSP and MAC EEPROM. Dedicated GPIOs drive the DSP reset (GPIO47), the BT **SYS_CTRL** (GPIO15) and the BT **RESET** (GPIO17).

3.5 Power Stage

An **AP63203WU-7** synchronous buck (fixed 3.3 V, **EN**=**VIN**, 100 nF bootstrap, 4.7 μ H inductor, 22 μ F output) generates the main rail from the USB-C input protected by a single **SS34** Schottky. A **TPS7A2018** low-noise LDO (**EN**=3.3 V) derives the 1.8 V rail. USB ESD is handled by an **SRV05-4** at the connector.

Chapter 4

PCB Design

4.1 Layer Stack-up

DigiRadio uses a 6-layer stack with two dedicated ground planes, so that sensitive RF and clock nets on the top layer reference a solid, uninterrupted ground plane immediately beneath (Figure 4.1).

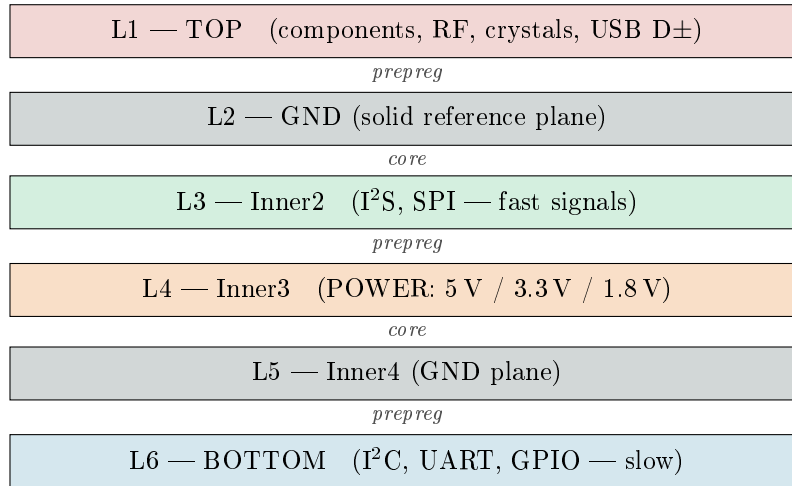


Figure 4.1: 6-layer stack-up. Fast signals (L3) are sandwiched between GND (L2) and POWER (L4); slow signals live on the bottom, referenced to the second GND plane (L5).

Design Decision

The stack is built around signal integrity, not routing convenience. The USB differential pair is routed on **TOP**, referenced to the L2 ground plane, where $90\ \Omega$ differential impedance is achievable at manufacturable trace widths (6 mil trace / 8 mil gap). Routing it on an inner layer through the thicker core would have required non-manufacturable trace widths.

4.2 Controlled Impedance

Net	Layer	Target	Geometry (PCBWay 6-layer)
USB D+/D-	TOP / ref L2	$90\ \Omega$ diff	6 mil trace, 8 mil gap
FM/DAB RF	TOP / ref L2	microstrip	short, in-line, no vias in path
I²S / SPI	Inner2	— (digital)	6 mil, GND-referenced

4.3 Plane Continuity and Keep-outs

The L2 ground plane is kept solid and unbroken under the RF trace, the two crystals and the USB pair; verification confirmed no plane splits or via “slots” in these regions. Three antenna zones are cleared of copper on *all* layers: the ESP32-S3 module antenna, the FSC-BT1035 module antenna, and the FM/DAB SMA trace. The two 2.4 GHz antennas (ESP32, BT1035) are placed diagonally to maximise separation.

Chapter 5

Interfaces and Bus Map

5.1 I²S Topology

The DSP is master; the Si4684 and FSC-BT1035 are slaves. BCLK and LRCLK are single nets shared by all I²S devices; each clock reaches every device that uses it (including both DSP serial ports).

Signal	Path
BCLK / LRCLK	ADAU1701 (master) → Si4684, FSC-BT1035, ESP32
SDATA_IN0	Si4684 → ADAU1701
SDATA_IN1	ESP32-S3 → ADAU1701
SDATA_OUT0	ADAU1701 → FSC-BT1035

5.2 I²C Address Map

A single system I²C bus (2.2 k Ω pull-ups to 3.3 V) hosts the DSP and the MAC EEPROM; the self-boot EEPROM is a DNP option.

Device	Address	Role
ADAU1701	0x68 (ADDR=00)	DSP control
24AA025E48	0x52	MAC / EUI-48 EEPROM
24LC256 (DNP)	0x50	optional self-boot EEPROM

5.3 Other Buses

Bus	Devices	Notes
SPI	Si4684	firmware/patch load + control; software CS
UART0	CN1 header	system monitor (native USB used for flashing)
UART1	FSC-BT1035	ASCII command set, 4-wire with flow control
USB	USB-C	native ESP32-S3 USB (GPIO19/20), SRV05-4 ESD

Chapter 6

Bill of Materials

Summary of the production BOM (41 line items, 83 placements). Passive values are grouped; see the machine-readable BOM in `Hardware/bom/` for the full list with manufacturer part numbers and designators.

Item	Value / Part	Qty
<i>Active devices</i>		
Si4684-A10-GM (tuner)	QFN-48	1
ADAU1701JSTZ-RL (DSP)	LQFP-48	1
FSC-BT1035 (Bluetooth)	module	1
ESP32-S3-WROOM-1-N16 (host)	module	1
AP63203WU-7 (buck)	TSOT-26	1
TPS7A2018 (LDO)	TSOT-23-5	1
24AA025E48 (EEPROM)	SOT-23-6	1
SRV05-4 (USB ESD)	SOT-23-6	1
SS34 (Schottky)	SMA	1
BAV99 (RF clamp)	SOT-23-3	1
<i>Crystals & inductors</i>		
19.2 MHz (Si4684 ref)	3225	1
12.288 MHz (DSP)	3225	1
4.7 μ H (buck)	SMD	1
18/22/120 nH (RF match)	0402	3
<i>Passives (grouped)</i>		
100 nF	0402	15
1 μ F	0402/0603	8
10 μ F	0805 (50 V)	7
22 μ F	0805 (25 V)	3
8.2 pF / 2.2 nF (C0G/X7R)	0402/0603	8
12 pF / 22 pF (xtal load, C0G)	0402	4
2.7 pF / 33 pF / 3.3 nF / 47 nF / 56 nF	0402	5
Resistors (100 Ω –10 k Ω , 475 Ω)	0402	13
<i>Connectors & switches</i>		
USB-C	SMD	1
SMA edge (FM/DAB)	TH	1
4-pin header (CN1)	2.54 mm	1
Tactile switches (EN/BOOT)	SMD	2

Chapter 7

Firmware Architecture (Planned)

The firmware is under active development and will be released after hardware bring-up. The planned architecture is given here as a specification.

Boot sequence. The ESP32-S3 (1) releases the DSP reset, (2) loads the SigmaStudio program into the ADAU1701 RAM over I²C, (3) starts the DSP core, (4) loads the Si4684 firmware/patch over SPI, and (5) brings up the FSC-BT1035 over UART.

Runtime control. Volume, EQ and source mix are written to the DSP safeload registers to avoid audio pops; DAB/FM tuning is commanded over SPI; A2DP source and aptX Adaptive are controlled over the BT UART.

Note

Multi-master safety: because the host controls the DSP reset, it knows exactly when it released it. It waits until the DSP program load completes before issuing further I²C traffic, so the single system bus never sees two active masters.

Chapter 8

Manufacturing

- **Fabrication:** 6-layer, 50×90 mm, PCBWay, with **impedance control** (USB $90\ \Omega$ differential on TOP referenced to L2; RF microstrip). Inner-layer copper 0.5 oz, outer 1 oz.
- **Assembly:** turnkey PCBA. Most parts are standard distributor stock.
- **FSC-BT1035 sourcing:** sourced from Feasycom (or authorised distributor). Specify in the order that U11 is a Feasycom FSC-BT1035 (QCC3056) and that the footprint uses a BT806-compatible land pattern.
- **MSL-3:** the FSC-BT1035 is moisture-sensitive level 3 — bake before reflow.
- **Antenna keep-outs:** three antenna zones must remain copper- and paste-free on all layers.

Appendix A

Design Review Notes

The following issues were identified and resolved during design review. They are recorded here both for transparency and as a reference for anyone building on the design.

Issue	Resolution
Crystal load caps	An automated value pass had set the 12.288 MHz load caps to 22 μ F instead of 22 pF (a fatal 10^6 error that would stop the DSP oscillator). Corrected to 22 pF C0G; the 19.2 MHz caps to 12 pF C0G.
DSP VDRIVE	Found tied to GND (digital outputs effectively dead); corrected to 3.3 V.
DSP PLL_MODE	PLL_MODE1 found high ($512 \times fs \rightarrow 24$ kHz); both pins set low for $256 \times fs$ (48 kHz).
Bulk capacitor derating	Bulk 10/22 μ F migrated to 0402/6.3 V lost most of their capacitance to DC bias (and 6.3 V on a 5 V input rail is unsafe); moved back to 0805 with adequate voltage rating.
I ² C multi-master	The DSP control port was isolated with its self-boot EEPROM instead of on the system bus; moved to the shared bus, and the host-load model adopted to keep a single master.
Si4684 bypass return	Supply bypass capacitors correctly return to DBYP/ABYP (not GND) per AN851.
USB impedance	Confirmed 90 Ω differential requires the pair on TOP referenced to L2, at 6 mil/8 mil, rather than an inner layer.
BT module identity	BOM label corrected from FSC-BT806 to FSC-BT1035 (QCC3056); the land pattern is pin-compatible.